PDF SOLUTIONS INC
Form 10-K/A
March 18, 2010

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UNITED STATES
SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

Form 10-K/A
Amendment No. 1

(Mark One)

ý **ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**

For the fiscal year ended December 31, 2009

or

o **TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**

For the transition period from to
000-31311
(Commission file number)

PDF SOLUTIONS, INC.

(Exact name of registrant as specified in its charter)

Delaware	**25-1701361**
(State or other jurisdiction of Incorporation or organization)	(I.R.S. Employer Identification No.)
333 West San Carlos Street, Suite 700 San Jose, California	**95110**
(Address of Registrant's principal executive offices)	(Zip Code)

(408) 280-7900

(Registrant's telephone number, including area code)

Securities registered pursuant to Section 12(b) of the Act:

Title of Class	Name of Each Exchange on Which Registered
Common Stock, $0.00015 par value	The NASDAQ Stock Market LLC

Securities registered pursuant to Section 12(g) of the Act:

None

Indicate by check mark if the registrant is a well-known seasoned issuer (as defined in Rule 405 of the Securities Act). Yes o No ý

Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act. Yes o No ý

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Act of 1934 during the preceding 12 months (or for such shorter period that the Registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes ý No o

Indicate by check mark whether the registrant has submitted electronically and posted on its corporate Web site, if any, every Interactive Data File required to be submitted and posted pursuant to Rule 405 of Regulation S-T (§ 232.405 of this chapter) during the preceding 12 months (or for such shorter period that the registrant was required to submit and post such files). Yes o No o

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K/A or any amendment to this Form 10-K/A. ý

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non-accelerated filer, or a smaller reporting company. See the definitions of "large accelerated filer," "accelerated filer" and "smaller reporting company" in Rule 12b-2 of the Exchange Act. (Check one):

Large accelerated filer o	Accelerated filer o	Non-accelerated filer o (Do not check if a smaller reporting company)	Smaller reporting company ý

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Act). Yes o No ý

The aggregate market value of the voting stock held by non-affiliates of the Registrant was approximately $48.5 million as of the last business day of the Registrant's most recently completed second quarter, based upon the closing sale price on the NASDAQ Global Market reported for such date. Shares of Common Stock held by each officer and director and by each person who owns 10% or more of the outstanding Common Stock have been excluded in that such persons may be deemed to be affiliates. This determination of affiliate status is not necessarily a conclusive determination for other purposes.

There were 26,965,998 shares of the Registrant's Common Stock outstanding as of March 5, 2010.

DOCUMENTS INCORPORATED BY REFERENCE

Part III incorporates certain information by reference from the definitive Proxy Statement for our Annual Meeting of Stockholders expected to be held on May 18, 2010.

EXPLANATORY NOTE

PDF Solutions, Inc. ("PDF" or the "Company") is filing this Amendment No. 1 on Form 10-K/A (this "Amendment") to amend the Company's Annual Report on Form 10-K for the year ended December 31, 2009, as filed with the Securities and Exchange Commission on March 16, 2010. Specifically, the purpose of this Amendment is to correct typographical errors in the Index to Consolidated Financial Statements and the Consolidated Statements of Cash Flows, each under Part IV, Item 15 "Exhibits and Financial Statement Schedules". The correction on the Consolidated Statements of Cash Flows was to change negative $8,485,000 to positive $8,485,000 for net cash provided by investing activities in 2009; and the correction to the Index to the Consolidated Financial Statements was to add year 2008 and 2007 to the lines Consolidated Statements of Operations, Consolidated Statements of Stockholders' Equity and Comprehensive Income (Loss), and Consolidated Statements of Cash Flows. This Amendment speaks as of the original filing date of PDF's Annual Report on Form 10-K. Except for this correction on the Index to Consolidated Financial Statements and the Consolidated Statements of Cash Flows, no other changes to the Annual Report on Form 10-K are being made by means of this filing. PDF is filing the entire Annual Report, as amended, for convenience of its investors.

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PART I

This Annual Report on Form 10-K/A, particularly in Item 1 "Business" and Item 7 "Management's Discussion and Analysis of Financial Condition and Results of Operations," includes forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 (the "Securities Act") and Section 21E of the Securities Exchange Act of 1934, as amended (the "Exchange Act"). These statements include, but are not limited to, statements concerning: expectations about the effectiveness of our business and technology strategies; expectations regarding stock market and global economic trends; expectations regarding previous and future acquisitions; current semiconductor industry trends; expectations of the success and market acceptance of our intellectual property and our solutions; expectations concerning recent completed acquisitions; expectations that our cash, cash equivalents and cash generated from operations will satisfy our business requirements for the next twelve months; expectations of our future liquidity requirements; and our ability to obtain additional financing when needed. Our actual results could differ materially from those projected in the forward-looking statements as a result of a number of factors, risks and uncertainties discussed in this Form 10-K/A, especially those contained in Item 1A of this Form 10-K/A. The words "may," "anticipate," "plan," "continue," "could," "projected," "expect," "believe," "intend," and "assume," the negative of these terms and similar expressions are used to identify forward-looking statements. All forward-looking statements and information included herein is given as of the filing date of this Form 10-K/A with the Securities and Exchange Commission ("SEC") and based on information available to us at the time of this report and future events or circumstances could differ significantly from these forward-looking statements. Unless required by law, we undertake no obligation to update publicly any such forward-looking statements.

The following information should be read in conjunction with the Consolidated Financial Statements and notes thereto included in this Annual Report on Form 10-K/A. All references to fiscal year apply to our fiscal year that ends on December 31.

Item 1. *Business*

Business Overview

PDF Solutions is a leading provider of infrastructure technologies and services to lower the cost of integrated circuit ("IC") design and manufacturing, enhance time to market, and improve profitability by addressing design and manufacturing interactions from product design to initial process ramps to mature manufacturing operations. Our technologies and services target the entire "process life cycle," which is the term we have coined for the time from the design of an IC through volume manufacturing of that IC. Our solutions combine proprietary software, physical intellectual property ("IP") in the form of cell libraries for IC designs, test chips, an electrical wafer test system, proven methodologies, and professional services. We analyze yield loss mechanisms to identify, quantify, and correct the issues that cause yield loss. Our analysis drives IC design and manufacturing improvements to enable our customers to optimize the technology development process, to increase initial yield when an IC design first enters a manufacturing line, to increase the rate at which yield improves, and to minimize excursions and process variability that cause yield loss throughout mass production. The result of successfully implementing our solutions is the creation of value that can be measured based on improvements to our customers' actual yield. Through our gainshare performance incentives component, we have aligned our financial interests with the yield and performance improvements realized by our customers, and we receive revenue based on this value. Our technologies and services have been sold to leading integrated device manufacturers, fabless semiconductor companies, and foundries.

The key benefits of our solutions to our customers are:

Faster Time to Market. Our solutions are designed to accelerate our customers' time-to-market and increase product profitability. Our solutions, which can predict and improve product yield even before IC product design is complete, transform the traditional design-to-silicon sequence into a primarily concurrent process, thereby shortening our customers' time-to-market. Systematically

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incorporating knowledge of the integration of the design and manufacturing processes into our software modules and physical IP enables our customers to introduce products with higher initial yields faster. Our solutions are designed to decrease design and process iterations and reduce our customers' up-front costs, and thus provide our customers with early-mover advantages such as increased market share and higher selling prices.

Faster Time to Volume. After achieving higher initial yields and faster time-to-market, our solutions are designed to enable our customers to isolate and eliminate remaining yield issues to achieve cost efficient volume manufacturing. Once a manufacturing process has been modeled using our solutions, our customers are able to diagnose problems and simulate potential corrections more quickly than using traditional methods. In addition, if process changes are required, improvements can be verified more quickly using our technology than using traditional methods. Our solutions thus enable our customers to quickly reach cost efficient volume, so that they are able to increase margins, improve their competitive position, and capture higher market share.

Increased Manufacturing Efficiencies. Our solutions for product design, product introduction, yield ramp, and process control are designed to allow our customers to achieve a higher yield at mass production and therefore a lower cost of goods sold. In addition, our solutions, which also include fault detection and classification ("FDC") software, are designed to provide our customers with the ability to proactively monitor process health to avoid potential yield problems.

Our long-term business objective is to maximize IC yield by providing the industry standard in technologies and services for the Process Life Cycle. To achieve this objective, we intend to:

Expand Strategic Relationships. We intend to continue to extend and enhance our relationships with companies at various stages of the design-to-silicon process, such as process licensors, manufacturing and test equipment vendors, electronic design automation vendors, silicon IP providers, semiconductor foundries, and contract test and assembly houses. For example, an agreement with International Business Machines Corporation ("IBM") to develop an IC design platform to mitigate the effects of escalating design and manufacturing process complexity at the 32-, 28-, and 22-nanometer (nm) dimensions enables us to layer our *pd*BRIX -based platform on top of IBM's world class manufacturing process so it can be used by a broad set of manufacturers and fabless firms.

Extend Our Technology Leadership Position. We intend to extend our technology leadership position by leveraging our experienced engineering staff and codifying the knowledge that we acquire in our solution implementations. For example, we continue to expand and develop new technology that leverages our Characterization Vehicle® (CV®) methodology to embed test structures on product wafers. This provides valuable insight regarding product yield loss during mass production with minimal or no increase in test time and non-product wafers. In addition, we selectively acquire complementary businesses and technologies to increase the scope of our solutions.

Leverage Our Gainshare Performance Incentives Business Model. We intend to continue expanding the gainshare performance incentives component of our customer contracts. We believe this approach allows us to form collaborative and longer-term relationships with our customers by aligning our financial success with that of our customers. Working closely with our customers on their core technologies that implement our solutions, with a common focus on their business results, provides direct and real-time feedback for continual improvement of our solutions. We believe that we will generate expanded relationships with customers that engage us on terms that include a significant gainshare performance incentive component.

Focus on Key IC Product Segments and High-Growth Adjacent Markets. We intend to focus our solutions on high-volume, high-growth IC product segments such as system-on-a-chip, memory,

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CMOS image sensor, and high-performance central processing units. As a result, we will continue to expand our solutions for technology drivers such as low-k dielectrics, high-k metal gates, immersion lithography, double patterning, SOI, copper, and 300mm wafer fabs, which are all still somewhat new and are relatively complex manufacturing technologies. We believe that these product segments are particularly attractive because they include complex IC design and manufacturing processes where processed silicon is costly and yield is critical. In addition, we have expanded our efforts to penetrate high growth adjacent markets, such as photovoltaic manufacturing. We are leveraging our yield management system and FDC technology to create products that meet the needs of manufacturing customers in the rapidly growing solar markets.

Industry Background

Rapid technological innovation, with increasingly shorter product life cycles, now fuels the economic growth of the semiconductor industry. IC companies historically ramped production slowly, produced at high volume once products gained market acceptance, and slowly reduced production volume when price and demand started to decrease near the end of the products' life cycles. Now, companies often need to be the first to market and the first to sell the most volume when a product is first introduced so that they have performance and pricing advantages over their competition, or else they lose market opportunity and revenue. Increased IC complexity and compressed product lifecycles create significant challenges to achieve competitive initial yields and optimized performance. For example, it is not uncommon for an initial manufacturing run to yield only 20%, which means that 80% of the ICs produced are wasted. Yield improvement and performance optimization are critical drivers of IC companies' financial results because they typically lead to cost reduction and revenue generation concurrently, causing a leveraged effect on profitability.

Technology and Intellectual Property Protection

We have developed proprietary technologies for yield simulation, analysis, loss detection, and improvement. The foundation for many of our solutions is our CV infrastructure ("CV*i*") that enables our customers to characterize the manufacturing process, and establish fail-rate information needed to calibrate manufacturing yield models, prioritize yield improvement activities and speed-up process learning-cycles. Our CV*i* includes proprietary Characterization Vehicle® test chips, including designs of experiments and layout designs, and a proprietary and patented highly parallel electrical functional and parametric-test system, comprised of hardware and software designed to provide an order-of-magnitude reduction in the time required to test our Characterization Vehicle® test chips. In addition, our technology embodies many algorithms, which we have developed over the course of many years, and which are implemented in our products including *data*POWER®, pdCV , mæstria®, and pdBRIX , among others. Further, our IP includes methodologies that our implementation teams use as guidelines to drive our customers' use of our CV® test chips and technologies, quantify the yield-loss associated with each process module and design block, simulate the impact of changes to the design and/or to the manufacturing process, and analyze the outcome of executing such changes. We continually enhance our core technologies through the codification of knowledge that we gain in our solution implementations.

Our future success and competitive position rely to some extent upon our ability to protect these proprietary technologies and IP, and to prevent competitors from using our systems, methods, and technologies in their products. To accomplish this, we rely primarily on a combination of contractual provisions, confidentiality procedures, trade secrets, and patent, copyright, mask work, and trademark laws. We license our products and technologies pursuant to non-exclusive license agreements that impose restrictions on customers' use. In addition, we seek to avoid disclosure of our trade secrets, including requiring employees, customers, and others with access to our proprietary information to execute confidentiality agreements with us and restricting access to our source code. We also seek to protect our software, documentation, and other written materials under trade secret and copyright laws. As of

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December 31, 2009, we held 42 U.S. patents. We intend to prepare additional patent applications when we feel it is necessary. Characterization Vehicle®, Circuit Surfer®, CV®, *dataPOWER*®, mæstria®, ModelWare®, Optissimo®, pdFasTest®, pDfx®, PDF Solutions®, Proxecco®, the PDF Solutions logo, Yield Ramp Simulator®, and YRS® are registered trademarks of PDF Solutions, Inc. or its subsidiaries, and Design-to-Silicon-Yield *dP*-bitMAP *dP*-Defect *dP*-Mining *dP*-probeMAP *dP*-shotMAP *dP*-SSA *dP*-Variability Analysis *dP*-VUE , *dP*-WorkFlow , pdBRIX , pdCV , and YA-FDC are our common law trademarks.

Products and Services

Our solutions consist of integration engineering services, proprietary software, and other technologies designed to address our customers' specific manufacturing and design issues.

Services and Solutions

Manufacturing Process Solutions ("MPS"). The IC manufacturing process typically involves four sequential phases: research and development to establish unit manufacturing processes, such as units for the metal CMP or lithography processes; integration of these unit processes into functional modules, such as metal or contact modules; a yield ramp of lead products through the entire manufacturing line; and volume manufacturing of all products through the life of the process. We offer solutions targeted to each of these phases designed to accelerate the efficiency of yield learning by shortening the learning cycle, learning more per cycle, and reducing the number of silicon wafers required. Our targeted offerings include:

Process R&D: Our process R&D solutions are designed to help customers increase the robustness of their manufacturing processes by characterizing and reducing the variability of unit processes and device performance with respect to layout characteristics within anticipated process design rules.

Process Integration and Yield Ramp: Our process integration and yield ramp solutions are designed to enable our customers to more quickly ramp the yield of new products early in the manufacturing process by characterizing the process-design interactions within each key process module, simulating product yield loss by process module, and prioritizing quantitative yield improvement by design block in real products.

Volume Manufacturing Solutions ("VMS"). Our volume manufacturing solutions are designed to enable our customers to extend our yield ramp services through the life of the process by continuing to collect test data and equipment signals during production and improving yield while reducing the overhead of manufacturing separate test wafers. They enable the customer to collect test data and equipment signals during production to improve yield while simultaneously reducing the overhead of manufacturing. Our dataPOWER® software modules allow customers to perform rapid yield signature detection, characterization, and diagnosis. Our mæstria® and YA-FDC process control software offerings enable our customers to monitor and control process signals to detect and diagnose yield loss related to equipment performance.

Design-for-Manufacturability ("DFM") Solutions. Our DFM solutions are designed to enable our customers to optimize yields, improve parametric performance, and reduce product ramp time by integrating manufacturability considerations into the design cycle before a design is sent to the mask shop to more quickly and cost-effectively manufacture IC products. We target these solutions to customers' requirements by providing the following:

Logic DFM Solutions: Logic DFM solutions include software, IP, and services designed to make yield improvements by trading off density or performance, for example, in the logic portions of an IC design. Our software helps designers optimize the yield of the logic portion by using process-

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specific yield models and technology files that include yield enhanced extensions to IP design building block elements.

Circuit Level DFM Solutions: Circuit level DFM solutions include software and services designed to anticipate the effects of process variability during analog/mixed signal/RF circuit design to optimize the manufacturability of each block given a pre-characterized manufacturing process.

Memory DFM Solutions: Memory DFM solutions include software and services designed to optimize the memory redundancy and bit cell usage given a pre-characterized manufacturing process.

pdBRIX Physical IP Solutions: pdBRIX physical IP solutions include software, IP and services for identifying and developing a set of layout patterns which we refer to as Templates that are optimized to a given manufacturing process and target product application. These Templates serve as the building blocks for design organizations to construct standard cell libraries and larger physical IP blocks which we refer to as Bricks. This solution includes mapping software for inserting these into a design flow.

Products

Our Manufacturing Process, Volume Manufacturing, and DFM solutions incorporate the use of various elements of our software products and other technologies, depending on the customers' needs. Our software products and other technologies include the following:

Characterization Vehicle® Infrastructure. Our test chip design engineers develop a design of experiments ("DOEs") to determine how IC design building blocks interact with the manufacturing process. Our CV software utilizes the DOE, as well as a library of building blocks that we know has potential yield and performance impact, to generate CV test chip layouts. Our CV infrastructure includes:

CV® Test Chips. Our family of proprietary test chip products is run through the manufacturing process with intentional process modifications to explore the effects of potential process improvements given natural manufacturing variations. Our custom-designed CV test chips are optimized for our test hardware and analysis software and include DOEs tuned to each customer's process. Our full-reticle short-flow CV test chips provide a fast learning cycle for specific process modules and are fully integrated with third-party failure analysis and inspection tools for complete diagnosis to root cause. Our Scribe CV® products are inserted directly on customers' product wafers and collect data from product wafers about critical layers.

pdCV Analysis Software. Our proprietary software accumulates data from our CV test chips, enabling models of the performance effects of process variations on these design building blocks to be generated for use with our Yield Ramp Simulator software.

pdFasTest® Electrical Wafer Test System. Our proprietary system enables fast defect characterization of manufacturing processes. This automated system provides parallel functional testing, thus minimizing the time required to perform millions of electrical measurements to test our CV test chips.

Yield Ramp Simulator® (YRS®) Software. Our YRS software analyzes an IC design to compute its systematic and random yield loss. YRS software allows design attribute extraction and feature-based yield modeling. YRS software takes as input a layout that is typically in industry standard format and proprietary yield models generated by running and testing our CV test chips. YRS software is designed to estimate the yield loss due to optical proximity effects, etch micro-loading, dishing in CMP, and other basic process issues.

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Circuit Surfer® Software. Our Circuit Surfer software estimates the parametric performance yield and manufacturability of analog/mixed-signal/RF blocks in a design, such as RF transmission, PLLs/DLLs and logic critical paths. Using our Circuit Surfer software, a design engineer is able to estimate how manufacturing process variations will impact circuit performance and yield and then optimizes the circuit to reduce or eliminate the impact of those variations.

pdBRIX Platform. Our pdBRIX platform includes software for identifying and developing a set of physical IP building blocks that are tailored to a given manufacturing process and target product application. This platform also includes mapper software for inserting these physical IP building blocks into a traditional design flow.

dataPOWER® YMS Platform. Our *data*POWER YMS platform collects yield data, loads and stores it in an integrated database and allows product engineers to identify and analyze production yield issues using proprietary yield analysis software tools. *data*POWER software contains powerful visualization and reporting tools, including web-based access through the *dP*-Monitor module included in the core product in the newest release, which are flexible to address customers' requirements. Our YMS platform is designed to handle very large data sets, to efficiently improve productivity, yield and time-to-market at our customers' sites. Optional modules extend the base platform to enable defect analysis (*dP*-Defect), memory analysis (*dP*-bitMAP), spatial signature analysis (*dP*-SSA), data-mining (*dP*-Mining), optimization of die on the wafer (*dP*-shotMAP), and probe-head optimization (*dP*-probeMAP), and web-based access (*dP*-VUE).

mæstria® FDC Software. Our mæstria product provides FDC capabilities to rapidly identify sources of process variations and manufacturing excursions by monitoring equipment parameters through proprietary data collection and analysis features.

YA-FDC Service and Software Platform. YA-FDC allows online modeling to create real-time virtual measurements of final product attributes during processing. These models enable optimization decisions for process control, process adjustments, PM scheduling, tool corrective actions, and wafer dispatching. The real-time decision-making based on the models is designed to reduce product variability and cost simultaneously.

With the exception of *data*POWER, mæstria and pdBRIX, the primary distribution method for our software and technologies is through our manufacturing process solutions although, we have in the past and may in the future separately license these and other technologies. Though *data*POWER, mæstria and pdBRIX are primarily licensed separately, they may also be distributed within our Design-to-Silicon-Yield solutions.

Customers

Our current customers are primarily integrated device manufacturers ("IDMs"), but also include fabless semiconductor design companies and foundries. Our customers' targeted product segments vary significantly, including microprocessors, memory, graphics, image sensor solutions, and communications. We believe that the adoption of our solutions by such companies for usage in a wide range of products validates the application of our Design-to-Silicon-Yield solutions to the broader semiconductor market.

IBM, Toshiba Corporation ("Toshiba"), and Chartered Semiconductor Manufacturing ("Chartered") represented 19%, 17%, and 11%, respectively, of our revenues for the year ended December 31, 2009. Toshiba and IBM represented 18% and 16%, respectively, of our revenues for the year ended December 31, 2008. Toshiba and IBM represented 19% and 16%, respectively, of our revenues for the year ended December 31, 2007. No other customer accounted for 10% or more of our revenues in 2009, 2008 and 2007.

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Sales and Marketing

Our sales strategy is to pursue targeted accounts through a combination of our direct sales force, sales representatives in some local markets, and strategic alliances. For sales in the United States, we rely on our direct sales team, which primarily operates out of our San Jose, California headquarters. In Europe, Japan, and Korea, we primarily use our direct sales team. In Taiwan, we use a combination of our direct sales team and a local sales representative, J.I.T. International Co., Ltd. In Singapore, Malaysia, and Indonesia, we use Kromax South Asia PTE LTD, a local sales representative. We expect to continue to establish strategic alliances with process licensors, vendors in the electronic design automation software, capital equipment for IC production, silicon IP and mask-making software segments to create and take advantage of sales channel and co-marketing opportunities.

After we are engaged by a customer and early in the solution implementation, our engineers seek to establish relationships in the organization and gain an understanding of our customers' business issues. Our direct sales and solution implementation teams combine their efforts to deepen our customer relationships by expanding our penetration across the customer's products, processes and technologies. This close working relationship with the customer has the added benefit of helping us identify new product areas and technologies in which we should next focus our research and development efforts.

In the year ended December 31, 2009, we derived 66% of our revenues from customers based in Asia compared to 55% in both of the years ended December 31, 2008 and 2007. In the year ended December 31, 2009, 27% of our revenues were derived from customers located in the United States as compared to 27% and 31%, respectively, in the years ended December 31, 2008 and 2007. Additional discussion regarding the risks associated with international operations can be found under Item 1A, "Risk Factors".

See our "Notes to Consolidated Financial Statements", included under Part II, Item 8. "Financial Statements and Supplementary Data" for additional geographic information.

Research and Development

Our research and development focuses on developing and introducing new proprietary technologies, software products and enhancements to our existing solutions. We use a rapid-prototyping paradigm in the context of the customer engagement to achieve these goals. We have made, and expect to continue to make, substantial investments in research and development. The complexity of our Design-to-Silicon-Yield technologies requires expertise in physical IC design and layout, transistor design and semiconductor physics, semiconductor process integration, numerical algorithms, statistics and software development. We believe that our team of engineers will continue to advance our market and technological leadership. We conduct in-house training for our engineers in the technical areas, as well as focusing on ways to enhance client service skills. At any given time, about one quarter of our research and development engineers are operating in the field, partnered with solution implementation engineers in a deliberate strategy to provide direct feedback between technology development and customer needs. Our research and development expenses were $19.8 million, $34.0 million and $36.1 million in 2009, 2008 and 2007, respectively.

Competition

The semiconductor industry is highly competitive and driven by rapidly changing design and process technologies, evolving standards, short product life cycles, and decreasing prices. While the market for process-design integration technologies and services is in its early stages, it is quickly evolving and we expect market competition to continue to develop and increase. We believe the solution to address the needs of IC companies requires a unified system of yield models, design analysis software, CV test chips, physical IP creation, process control software, and yield management software. Currently, we are the only provider of comprehensive commercial solutions for integrating design and manufacturing processes. We face indirect competition from internal groups at IC companies that use an incomplete set of components

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not optimized to accelerate process-design integration. Some providers of yield management software, inspection equipment, electronic design automation, or design IP may seek to broaden their product offerings and compete with us.

We face competition for some of the point applications of our solutions including some of those used by the internal groups at IC companies. Specifically there are several suppliers of yield management and/or prediction systems, such as KLA-Tencor, MKS Instruments, Inc. ("MKS") (through its acquisition of Yield Dynamics, Inc.), Mentor Graphics (through its acquisition of Ponte Solutions), Synopsys, Inc. ("Synopsys"), and process control software, such as Applied Materials, Inc. (through its acquisition of the software division of Brooks Automation, Inc.), BISTel Inc., and Trancom Technology, Inc., and MKS. ARM Ltd. and Virage Logic Corporation provide standard cells in the physical IP space and Tela provides software for standard cell synthesis, each of which could compete with our pdBRIX solution. In addition, Synopsys now appears to offer directly competing DFM solutions, while other EDA suppliers provide alternative DFM solutions that may compete for the same budgetary funds.

We believe the principal factors affecting competition in our market include demonstrated results and reputation, strength of core technology, ability to create innovative technology, and ability to implement solutions for new technology and product generations. We believe that our solutions compete favorably with respect to these factors.

Employees

As of December 31, 2009, we had 306 employees worldwide, including 171 on client service teams, 75 in research and development, 29 in sales and marketing, and 31 in general and administrative functions. Of these employees, 143 are located in the US, 112 in Asia, and 51 in Europe. Worldwide, we had 375 employees as of December 31, 2008 and 382 as of December 31, 2007.

None of our employees are represented by a labor union. Our employees in France and Italy are subject to collective bargaining agreements in those countries. We believe our relationship with our employees is good.

Executive Officers

The following table and notes set forth information about our current executive officers as of March 15, 2010.

Name	Age	Position
John K. Kibarian, Ph.D.	46	President, Chief Executive Officer, and Director
Joy E. Leo	49	Chief Administration Officer
Keith A. Jones	39	Chief Financial Officer and Vice President, Finance(1)
David A. Joseph	56	Chief Strategy Officer
Cees Hartgring, Ph.D.	56	Vice President, Client Services and Sales
Kimon Michaels, Ph.D.	43	Vice President, Design for Manufacturability, and Director

(1) As reported in a Current Report on Form 8-K filed by us on March 5, 2010, Mr. Jones resigned as our Chief Financial Officer and Vice President, Finance on March 1, 2010, to be effective on March 17, 2010 following the filing of this Annual Report.

John K. Kibarian, Ph.D., one of our founders, has served as President since November 1991 and has served as our Chief Executive Officer since July 2000. Dr. Kibarian has served as a director since December 1992. Dr. Kibarian received a B.S. in Electrical Engineering, an M.S. E.C.E. and a Ph.D. E.C.E. from Carnegie Mellon University.

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Joy E. Leo has served as Chief Administration Officer since July 2008. Prior to joining PDF, Ms. Leo served as Senior Vice President, Chief Financial Officer and Secretary for Credence Systems Corporations, now known as LTX-Credence, a provider of focused, cost-optimized ATE solutions. Ms. Leo served as Vice President of Finance and Administration, Chief Financial Officer and Secretary for Artisan Components, Inc., now known as ARM Holdings PLC. Ms. Leo also served as Vice President of Finance and Administration and Chief Financial Officer for IMP, Inc., as Vice President of Finance, Operations and Administration for Innomedia Incorporated, and Vice President and Chief Financial Officer for Philips Components, a multi-billion dollar division of Royal Philips Electronics N.V. Ms. Leo received a B.A. in Business Administration and Finance from the University of Utah.

Keith A. Jones has served as Chief Financial Officer and Vice President, Finance since January 2006. Mr. Jones served as Director of Finance and SEC Compliance from July 2003 to December 2005. Prior to joining PDF, Mr. Jones served as Assistant Controller for Interwoven, Inc., a provider of enterprise content management solutions, and as Controller for eTime Capital, Inc., a financial software applications company. Prior to that, Mr. Jones served in various positions at Deloitte & Touche LLP, most recently as an Audit Manager. Mr. Jones received a B.S. in Business Administration from California State University, Fresno and is a Certified Public Accountant.

David A. Joseph has served as Chief Strategy Officer since April 2003. Mr. Joseph served as Executive Vice President Sales, Marketing, and Business Development from August 2001 through March 2003, as Vice President, Products and Methods from July 1999 through August 2001 and as Vice President, Business Development from November 1998 through June 1999. Prior to joining PDF, Mr. Joseph served KLA-Tencor, a semiconductor manufacturing company, in various positions, including Japan Business Manager, Vice President Customer Satisfaction and General Manager of Yield Analysis Software. Mr. Joseph received a B.S. in Mathematical Science from Stanford University.

Cees Hartgring, Ph.D., has served as Vice President, Client Services and Sales since June 2007. Dr. Hartgring served as Vice President and General Manager, Manufacturing Process Solutions from January 2004 through May 2007, as Vice President, Worldwide Sales and Strategic Business Development from April 2003 through December 2003 and as Vice President of Sales from September 2002 through March 2003. Prior to joining PDF, Dr. Hartgring served as President and Chief Executive Officer of Trimedia Technologies, a Philips Semiconductor spinout. Dr. Hartgring also held various executive positions at Philips Semiconductor, most recently as Vice President and General Manager of the Trimedia business unit. Dr. Hartgring received an undergraduate degree from the Technical University Delft and an M.S.E.E. and a Ph.D. in Electrical Engineering and Computer Science from the University of California at Berkeley.

Kimon Michaels, Ph.D., one of our founders, has served as Vice President, Design for Manufacturability since June 2007. Dr. Michaels served as Vice President, Field Operations for Manufacturing Process Solutions from January 2006 through May 2007, and has been a Director since November 1995. From March 1993 through December 2005, he served in various vice presidential capacities. He also served as Chief Financial Officer from November 1995 to July 1998. Dr. Michaels received a B.S. in Electrical Engineering, an M.S. E.C.E. and a Ph.D. E.C.E. from Carnegie Mellon University.

Available Information

We file or furnish various reports, such as registration statements, periodic and current reports, proxy statements and other materials with the SEC. Our Internet website address is www.PDF.com. You may obtain, free of charge on our Internet website, copies of our annual reports on Form 10-K, quarterly reports on Form 10-Q, current reports on Form 8-K, and amendments to those reports filed or furnished pursuant to Section 13(a) or 15(d) of the Exchange Act, as soon as reasonably practicable after we electronically file such material with, or furnish it to, the SEC. The information we post is intended for

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reference purposes only; none of the information posted on our website is part of this report or incorporated by reference herein.

In addition to the materials that are posted on our website, you may read and copy any materials we file with the SEC at the SEC's Public Reference Room at 100 F Street, NE, Washington, DC 20549-0120. You may obtain information on the operation of the Public Reference Room by calling the SEC at 1-800-SEC-0330. The SEC also maintains a Web site (http://www.sec.gov) that contains reports, proxy and information statements and other information regarding issuers, such as us, that file electronically with the SEC.

Item 1A. Risk Factors.

The semiconductor market is volatile and unpredictable, which limits our ability to forecast our business and could negatively impact our results of operations.

The semiconductor industry experienced significant challenges in 2008 and 2009 as a result of the decline in the macroeconomic environment. As a provider to global semiconductor companies, we are subject to business cycles, the timing, length and volatility of which can be difficult to predict. The semiconductor industry historically has been cyclical due to sudden changes in customers' manufacturing capacity requirements and spending, which depend in part on capacity utilization, demand for customers' integrated circuit ("IC") products, inventory levels relative to demand, and access to affordable capital. These changes have affected the timing and amounts of customers' purchases and investments in our Design-to-Silicon-Yield solutions, and continue to affect our sales, operating expenses and net income. If we are not able to make adjustments to our business quickly to appropriately align our cost structure with prevailing market conditions in periods of low demand, or if we do not have sufficient resources to meet customers' demands in periods of high demand, results could be negatively impacted and could differ greatly from our expectations.

We generate a large percentage of our revenues from a limited number of customers, so decreased volumes at any one of these customers, or the loss of any one of these customers could significantly reduce our revenue and results of operations below expectations.

Historically, we have had a small number of large customers for our core Design-to-Silicon-Yield solutions and we expect this to continue in the near term. In the year ended December 31, 2009, three customers accounted for 47% of our revenues, with IBM representing 19%, Toshiba representing 17%, and Chartered representing 11%. In the year ended December 31, 2008, two customers accounted for 34% of our revenues, with Toshiba representing 18% and IBM representing 16%. We could lose a customer due to its decision not to engage us on future process nodes, its decision not to develop its own future process node, or as a result of industry consolidation. The loss of any of these customers or a decrease in the sales volumes of their products could significantly reduce our total revenue below expectations. In particular, such a loss could cause significant fluctuations in results of operations because our expenses are fixed in the short term and it takes us a long time to replace customers.

If semiconductor designers and manufacturers do not continue to adopt, or they significantly delay adoption of, our Design-to-Silicon-Yield solutions, our revenues will suffer.

If semiconductor designers and manufacturers do not continue to adopt our Design-to-Silicon-Yield solutions, both as currently comprised and as we may offer them in the future, our revenues will decline. We may not be successful if we do not continue to enter into agreements with existing customers and new customers that cover a larger number of IC products and processes. If we do not develop new customer relationships with companies that are integrated device manufacturers ("IDMs"), fabless semiconductor companies, and foundries, as well as system manufacturers, the market acceptance of our solutions will

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suffer. Factors that may limit adoption of our Design-to-Silicon-Yield solutions by semiconductor companies include:

- our existing and potential customers' delay in their adoption of the next process technology;
- IDMs of logic ICs discontinuing or significantly cutting back their investment in the development of new process technology as a result of a shift to a model of outsourcing a larger proportion, or all, of the mass production of their ICs;
- our inability to keep pace with the rapidly evolving technologies and equipment used in the semiconductor design and manufacturing processes;
- our customers' failure to achieve satisfactory yield improvements using our Design-to-Silicon-Yield solutions;
- fewer processes being developed at our customers and, therefore, a reduction in the potential impact our solutions can add across at any single customers; and
- our inability to develop, market, or sell effective solutions that are outside of our traditional logic focus of manufacturing process solutions.

Our business is subject to risks associated with the ongoing financial crisis and weak global economy.

The severe tightening of the credit markets, turmoil in the financial markets, and weakened global economy which began in 2008 deteriorated in early 2009, and may not improve or could even worsen in 2010, contributed to slowdowns in the semiconductor industry, which impacts our ability to make sales. The markets for semiconductors depend largely on consumer spending. Economic uncertainty exacerbates negative trends in consumer spending and may cause some of our customers to delay or refrain altogether from entering into new engagements, licensing new or additional software products, or renewing maintenance and support for existing licensed software at historical levels. This will negatively affect our revenues. Difficulties in obtaining capital and deteriorating market conditions may also lead to the inability of some customers to obtain affordable financing for other purchases, which could tie up funds otherwise budgeted for purchases of our solutions and technologies. Customers with liquidity issues may also lead to additional bad debt expense. Further, these conditions and uncertainty about future economic conditions make it challenging for us to forecast our operating results, make business decisions, and identify the risks that may affect our business, financial condition and results of operations. If we are not able to timely and appropriately adapt to changes resulting from the difficult macroeconomic environment, our business, financial condition, and results of operations may be significantly negatively affected.

Revenues from our gainshare performance incentives is dependent on factors outside of our control, including the volume of ICs that our customers are able to sell to their customers.

Our gainshare performance incentives fee component ties the profits of our customers to our own. Through this component, revenues for a particular product is largely determined by the volume of that product that our customer is able to sell to its customers, which is outside of our control. Decreased demand for semiconductor products decreases the volume of products our customers are able to sell, which directly decreases our gainshare performance incentives revenues. Important factors that could cause demand for semiconductor products to negatively fluctuate include:

- changes in business and economic conditions, including the current downturn in the semiconductor industry and the overall economy; and
- decreases in consumer confidence caused by changes in market conditions, including changes in the credit market.

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Also, our customers may unilaterally decide to implement changes to their manufacturing processes during the period that is covered by gainshare performance incentives, which could negatively affect yield results. Since we currently work on a small number of large projects, any product that does not achieve commercial viability or a significant increase in yield, or sustain significant volume manufacturing during the time we receive gainshare performance incentives, revenues from such customers could significantly reduce our revenue and results of operations below expectations. In addition, if we work with two directly competitive products, volume in one may offset volume, and thus any of our related gainshare performance incentives, in the other product.

We may not be able to effectively implement our restructuring plans, and our restructuring plans may not result in the expected benefits on our planned schedule, or at all, which could negatively impact our future results of operations.

During the year ended December 31, 2008, we have implemented restructuring plans in an effort to align our cost structure with expected revenue. We may not be able to successfully complete and realize the expected benefits of our restructuring plans, such as improvements in operating margins and cash flows, in the restructuring periods contemplated or at all. The restructuring plans may involve higher costs or a longer timetable than we currently anticipate, mainly due to the timing and execution of some plans and programs subject to local labor law requirements, and consultation with appropriate work councils. Our inability to realize these benefits may result in an inefficient business structure that could negatively impact our results of operations. We also expect our restructuring plans to cause us to incur substantial costs related to severance and other employee-related costs. Our restructuring plans may also subject us to litigation risks and expenses. In addition, our restructuring plans may have other consequences, such as attrition beyond our planned reduction in workforce or a negative impact on employee morale, and our competitors may seek to gain a competitive advantage over us. The restructuring plans could also cause our remaining employees to be less productive, which in turn may negatively affect our revenue and other operating results in the future.

If we do not effectively manage, support, and safeguard our worldwide information systems, and integrate recent and planned growth, our business strategy may fail.

We have experienced in the past, and may experience in the future, interruptions in our information systems on which our global operations depend. Further, we may face attempts by others to gain unauthorized access through the Internet to our information technology systems or IP, which we may be unable to prevent. We could be unaware of an incident or its magnitude and effects until after it is too late to prevent it and the damage it may cause. The theft or unauthorized use or publication of our trade secrets and other confidential business information as a result of such an incident could negatively affect our competitive position, the value of our investment in product or research and development, and third parties might assert against us or our customers claims related to resulting losses of confidential or proprietary information or end-user data and/or system reliability. In any such event, our business could be subject to significant disruption, and we could suffer monetary and other losses, including reputational harm. Further, intentional hacking of, interference with physical damage to, failure of, or digital damage (such as significant viruses or worms) to, our information systems could disrupt and delay time-sensitive services or computing operations that we perform for our customers, which could negatively impact our business results and reputation. In addition, we must frequently expand our internal information system to meet increasing demand in storage, computing and communication. Our internal information system is expensive to expand and must be highly secure due to the sensitive nature of our customers' information that we transmit. Building and managing the support necessary for our growth places significant demands on our management and resources. These demands may divert these resources from the continued growth of our business and implementation of our business strategy. Further, we must adequately train our new personnel, especially our client service and technical support personnel, to effectively and accurately,

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respond to and support our customers. If we fail to do this, it could lead to dissatisfaction among our customers, which could slow our growth.

It typically takes us a long time to sell our unique solutions to new customers and into new markets, and that can result in uncertainty and delays in generating revenues.

Our gainshare performance incentives business model is unique and our Design-to-Silicon-Yield solutions are often unfamiliar to new customers. This results in a lengthier sales cycle compared to some of our competitors and requires a significant amount of our senior management's time and effort. Furthermore, we need to target those individuals within a customer's organization who have overall responsibility for the profitability of an IC. These individuals tend to be senior management or executive officers. We may face difficulty identifying and establishing contact with such individuals. Even after initial acceptance, due to the complexity of structuring the gainshare performance incentives component, the negotiation and documentation processes can be lengthy. It can take nine months or more to reach a signed contract with a customer. Unexpected delays in our sales cycle could cause our revenues to fall short of expectations. By way of example, one of the industries that we have recently targeted that we believe would greatly benefit from our yield management system and FDC technology is the rapidly growing solar panel industry. Our efforts to leverage our products in this industry may not be successful. Further, ongoing negotiations and evaluation projects with photovoltaic manufacturers may not result in significant revenues for us if we are unable to close new engagements in these markets on terms favorable to us, in a timely manner, or at all, or if we are unable to successfully deliver our products and services to such markets.

Our stock price may be volatile, and our common stock could decline in value, increasing potential dilution to our stockholders, or we may be delisted from the NASDAQ Global Market.

Our stock price has fluctuated widely during the last few years, from a low closing price of $0.97 per share during March 2009 to a high closing price of $19.36 per share during April 2006. This significant reduction in our stock price negatively impacts our ability to raise equity capital in the public markets and increases the cost to us, as measured by dilution to our existing shareholders, of equity financing. In addition, the reduced stock price also increases the cost to us, in terms of dilution, of using our equity for employee compensation or for acquisitions of other businesses. Additionally, in order for our common stock to continue to be quoted on the NASDAQ Global Market ("NASDAQ"), we must satisfy various listing maintenance standards established by NASDAQ, including, among other things, the general requirement that our stock price consistently trades at or above $1.00 per share and that the total market value of our common stock exceed $50,000,000. We have had in the past, and may have again in the future, periods when our stock does not trade at, or the market value of our common stock has been below, the levels required by NASDAQ rules. If we were to be delisted from the NASDAQ and move to an alternative market, which may be less efficient and less broad-based, we may have difficulty accessing capital markets for additional funding, and the ability of our stockholders to sell any of our common stock at all would be severely, if not completely, limited, which could cause our stock price to decline further. Delisting could also have other negative results, including the potential loss of confidence by employees, the loss of institutional investor interest, and fewer business development opportunities. Also, significant volatility in the stock price could be followed by a securities class action lawsuit, which could result in substantial costs and a diversion of our management's attention and resources.

If we fail to protect our intellectual property ("IP") rights, customers or potential competitors may be able to use our technologies to develop their own solutions which could weaken our competitive position, reduce our revenue, or increase our costs.

Our success depends largely on the proprietary nature of our technologies. We currently rely primarily on contractual, patent, copyright, trademark, and trade secret protection. Our pending patent applications

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may not result in issued patents, and even if issued, they may not be sufficiently broad to protect our proprietary technologies. Litigation may be necessary from time to time to enforce our IP rights or to determine the validity and scope of the proprietary rights of others. As a result of any such litigation, we could lose our proprietary rights and incur substantial unexpected operating costs. Litigation could also divert our resources, including our managerial and engineering resources.

Our solution implementations may take longer than we anticipate, which could cause us to lose customers and may result in adjustments to our operating results.

Our solution implementations require a team of engineers to collaborate with our customers to address complex yield loss issues by using our software and other technologies. We must estimate the amount of time needed to complete an existing solution implementation in order to estimate when the engineers will be able to commence a new solution implementation. In addition, our accounting for solution implementation contracts, which generate fixed fees, sometimes require adjustments to profit and loss based on revised estimates during the performance of the contract. These adjustments may have a material effect on our results of operations in the period in which they are made. The estimates giving rise to these risks, which are inherent in fixed-price contracts, include the forecasting of costs and schedules, and contract revenues related to contract performance.

If we are not able to attract, retain, motivate, and strategically locate talented employees, including some key executives, our business may suffer.

Our success and competitiveness depend on our ability to attract, retain, motivate, and strategically locate in our offices around the globe talented employees, including some of our key executives. Achieving this objective may be difficult due to many factors, including fluctuations in global economic and industry conditions, changes in our management or leadership, the hiring practices at our competitors or customers, cost reduction activities, and the effectiveness of our compensation programs, including equity-based programs. Further, we have had, and expect to continue to have, difficulty in obtaining visas permitting entry for some of our employees that are foreign nationals into the United States, and delays in obtaining visas permitting entry into other key countries, for several of our key personnel, which disrupts our ability to strategically locate our personnel. If we lose the services of any of our key executives or a significant number of our engineers, it could disrupt our ability to implement our business strategy. If we do not successfully attract, retain, and motivate key employees, including key executives, we may be unable to realize our business objectives and our operating results may suffer.

Competition in the market for yield improvement solutions and increased integration between IC design and manufacturing may intensify in the future, which could impede our ability to grow or execute our strategy.

Competition in our market may intensify in the future, which could slow our ability to grow or execute our strategy and could lead to increased pricing pressure. Our current and potential customers may choose to develop their own solutions internally, particularly if we are slow in deploying our solutions or improving them to meet market needs. Many of these companies have the financial and technical capability to develop their own solutions. Also, competitors may be able to operate with a lower cost structure than our engineering organization, which would give any such competitor's products a competitive advantage over our solutions. There may be other providers of commercial solutions for systematic IC yield and performance enhancement of which we are not aware. We currently face indirect competition from the internal groups at IC companies and some direct competition from providers of yield management or prediction software such as KLA-Tencor, MKS Instruments, Inc. ("MKS"), and Synopsys, Inc., and process control software, such as Applied Materials, Inc., BISTel Inc., and Trancom Technology, Inc., and MKS. Further, ARM Ltd. and Virage Logic Corporation provide standard cells in the physical IP space and Tela provides software for standard cell synthesis, each of which could compete with our pdBRIX solution. In

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addition, electronic design automation suppliers provide alternative DFM solutions that may compete for the same budgetary funds. Some providers of yield management software or inspection equipment may seek to broaden their product offerings and compete with us. In addition, we believe that the demand for solutions that address the need for better integration between the silicon design and manufacturing processes may encourage direct competitors to enter into our market. For example, large integrated organizations, such as IDMs, electronic design automation software providers, IC design service companies or semiconductor equipment vendors, may decide to spin-off a business unit that competes with us. Other potential competitors include fabrication facilities that may decide to offer solutions competitive with ours as part of their value proposition to their customers. If these potential competitors change the pricing environment or are able to attract industry partners or customers faster than we can, we may not be able to grow and execute our strategy as quickly or at all. In addition, customer preferences may shift away from our solutions as a result of the increase in competition.

We face operational and financial risks associated with international operations that could negatively impact our revenue.

We have in the past expanded our non-U.S. operations and may in the future continue such expansion by establishing overseas subsidiaries, offices, or contractor relationships in locations, if and when, deemed appropriate by our management. Thus, the success of our business is subject to risks inherent in doing business internationally, including in particular:

some of our key engineers and other personnel are foreign nationals and they may have difficulty gaining access to the United States and other countries in which our customers or our offices may be located and it may be difficult for us to recruit and retain qualified technical and managerial employees in foreign offices;

greater difficulty in collecting account receivables resulting in longer collection periods;

language and other