PDF SOLUTIONS INC
Form 10-K
March 14, 2014

UNITED STATES SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

Form 10-K

(Mark One)
ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934
For the fiscal year ended December 31, 2013

or
TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934
For the transition period from to

000-31311

(Commission file number)

PDF SOLUTIONS, INC.

(Exact name of registrant as specified in its charter)

Delaware	**25-1701361**
(State or other jurisdiction of	*(I.R.S. Employer*
Incorporation or organization)	*Identification No.)*
333 West San Carlos Street, Suite 1000	**95110**
San Jose, California	*(Zip Code)*
(Address of Registrant's principal executive offices)	

(408) 280-7900

(Registrant's telephone number, including area code)

Securities registered pursuant to Section 12(b) of the Act:

Title of Class	**Name of Each Exchange on Which Registered**
Common Stock, $0.00015 par value	The NASDAQ Stock Market LLC

Securities registered pursuant to Section 12(g) of the Act:

None

Indicate by check mark if the registrant is a well-known seasoned issuer (as defined in Rule 405 of the Securities Act). Yes No

Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act. Yes No

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Act of 1934 during the preceding 12 months (or for such shorter period that the Registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes No

Indicate by check mark whether the registrant has submitted electronically and posted on its corporate Web site, if any, every Interactive Data File required to be submitted and posted pursuant to Rule 405 of Regulation S-T (§ 232.405 of this chapter) during the preceding 12 months (or for such shorter period that the registrant was required to submit and post such files). Yes No

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of registrant’s knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K.

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non-accelerated filer, or a smaller reporting company. See the definitions of “large accelerated filer,” “accelerated filer” and “smaller reporting company” in Rule 12b-2 of the Exchange Act. (Check one):

Large accelerated filer Accelerated filer Non-accelerated filer Smaller reporting company
(Do not check if a smaller reporting company)

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Act). Yes No

The aggregate market value of the voting stock held by non-affiliates of the Registrant was approximately $346.7 million as of the last business day of the Registrant’s most recently completed second quarter, based upon the closing sale price on the NASDAQ Global Market reported for such date. Shares of Common Stock held by each officer and director and by each person who owns 10% or more of the outstanding Common Stock have been excluded in that such persons may be deemed to be affiliates. This determination of affiliate status is not necessarily a conclusive determination for other purposes.

There were 30,584,896 shares of the Registrant’s Common Stock outstanding as of March 10, 2014.

DOCUMENTS INCORPORATED BY REFERENCE

Part III incorporates certain information by reference from the definitive Proxy Statement to be filed within 120 days from December 31, 2013.

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SPECIAL NOTE REGARDING FORWARD LOOKING STATEMENTS

This Annual Report on Form 10-K, particularly in Item 1 "Business" and Item 7 "Management's Discussion and Analysis of Financial Condition and Results of Operations," includes forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 (the "Securities Act") and Section 21E of the Securities Exchange Act of 1934, as amended (the "Exchange Act"). These statements include, but are not limited to, statements concerning: expectations about the effectiveness of our business and technology strategies; expectations regarding stock market and global economic trends; expectations regarding previous and future acquisitions; current semiconductor industry trends; expectations of the success and market acceptance of our intellectual property and our solutions; expectations that our cash, cash equivalents and cash generated from operations will satisfy our business requirements for the next twelve months; expectations of our future liquidity requirements; and our ability to obtain additional financing when needed. Our actual results could differ materially from those projected in the forward-looking statements as a result of a number of factors, risks and uncertainties discussed in this Form 10-K, especially those contained in Item 1A of this Form 10-K. The words "may," "anticipate," "plan," "continue," "could," "projected," "expect," "believe," "intend," a negative of these terms and similar expressions are used to identify forward-looking statements. All forward-looking statements and information included herein is given as of the filing date of this Form 10-K with the Securities and Exchange Commission ("SEC") and based on information available to us at the time of this report and future events or circumstances could differ significantly from these forward-looking statements. Unless required by law, we undertake no obligation to update publicly any such forward-looking statements.

The following information should be read in conjunction with the Consolidated Financial Statements and notes thereto included in this Annual Report on Form 10-K. All references to fiscal year apply to our fiscal year that ends on December 31. All references to "we", "us", "our", "PDF", "PDF Solutions" or "the Company" refer to PDF Solutions, I

PART I

Item 1. ***Business***

Business Overview

PDF Solutions is a leading provider of infrastructure technologies and services to lower the cost of integrated circuit ("IC") design and manufacturing, enhance time to market, and improve profitability by addressing design and

manufacturing interactions from technology development and product design to initial process ramps and mature manufacturing operations. Our technologies and services target the entire "process life cycle," which is the term we have coined for the time from technology development and the design of an IC through volume manufacturing of that IC. Our solutions combine proprietary software, physical intellectual property in the form of cell libraries for IC designs, test chips, an electrical wafer test system, proven methodologies, and professional services. We analyze yield loss mechanisms to identify, quantify, and correct the issues that cause yield loss. Our analysis drives IC design and manufacturing improvements to enable our customers to optimize the technology development process, to increase initial yield when an IC design first enters a manufacturing line, to increase the rate at which yield improves, and to minimize excursions and process variability that cause yield loss throughout mass production. The result of successfully implementing our solutions is the creation of value that can be measured based on improvements to our customers' actual yield. Through our Gainshare performance incentives component, we have aligned our financial interests with the yield and manufacturing efficiency realized by our customers, and we receive revenue based on this value. Our technologies and services have been sold to leading integrated device manufacturers, fabless semiconductor companies, and foundries.

The key benefits of our solutions to our customers are:

Faster Time to Market. Our solutions are designed to accelerate our customers' time-to-market and increase product profitability. Our solutions, which can predict and improve product yield even before IC product design is complete, transform the traditional design-to-silicon sequence into a primarily concurrent process, thereby shortening our customers' time-to-market. Systematically incorporating knowledge of the integration of the design and manufacturing processes into our software modules and physical IP enables our customers to introduce products with higher initial yields faster. Our solutions are designed to decrease design and process iterations and reduce our customers' up-front costs, and thus provide our customers with early-mover advantages such as increased market share and higher selling prices.

Faster Time to Volume. After achieving higher initial yields and faster time-to-market, our solutions are designed to enable our customers to isolate and eliminate remaining yield issues to achieve cost efficient volume manufacturing. Once a manufacturing process has been modeled using our solutions, our customers are able to diagnose problems and simulate potential corrections more quickly than using traditional methods. In addition, if process changes are required, improvements can be verified more quickly using our technology than using traditional methods. Our solutions thus enable our customers to quickly reach cost efficient volume, so that they are able to increase margins, improve their competitive position, and capture higher market share.

Increased Manufacturing Efficiencies. Our solutions for product design, product introduction, yield ramp, and process control are designed to allow our customers to achieve a higher yield at mass production and therefore a lower cost of goods sold. In addition, our solutions, which also include fault detection and classification ("FDC") software, are designed to provide our customers with the ability to proactively monitor process health to avoid potential yield problems.

Our long-term business objective is to maximize IC yield by providing the industry standard in technologies and services for the Process Life Cycle. To achieve this objective, we intend to:

Extend Our Technology Leadership Position. We intend to extend our technology leadership position by leveraging our experienced engineering staff and codifying the knowledge that we acquire in our solution implementations. For example, we continue to expand and develop new technology that leverages our Characterization Vehicle® (CV®) methodology to embed test structures on product wafers. This provides valuable insight regarding product yield loss during mass production with minimal or no increase in test time and non-product wafers. In addition, we invest in research and development and selectively acquire complementary businesses and technologies to increase the scope of our solutions.

Leverage Our Gainshare Performance Incentives Business Model. We intend to continue expanding the Gainshare performance incentives component of our customer contracts. We believe this approach allows us to form collaborative and longer-term relationships with our customers by aligning our financial success with that of our customers. Working closely with our customers on their core technologies that implement our solutions, with a common focus on their business results, provides direct and real-time feedback for continual improvement of our solutions. We believe that we will generate expanded relationships with customers that engage us on terms that include a significant Gainshare performance incentive component.

Focus on Key IC Product Segments and High-Growth Adjacent Markets. We intend to focus our solutions on high-volume, high-growth IC product segments such as system-on-a-chip, memory, CMOS image sensor, and high-performance central processing units. As a result, we will continue to expand our solutions for technology drivers such as low-k dielectrics, high-k metal gates, immersion lithography, double patterning, SOI, Finfets, and 300mm wafer fabs. We believe that these product segments are particularly attractive because they include complex IC design and manufacturing processes where processed silicon is costly and yield is critical. In addition, we continue to consider opportunities in adjacent markets where we could leverage our solutions to meet the needs of these markets.

Expand Strategic Relationships. We intend to continue to extend and enhance our relationships with companies at various stages of the design-to-silicon process, such as process licensors, manufacturing and test equipment vendors, electronic design automation vendors, silicon IP providers, semiconductor foundries, and contract test and assembly houses.

Brief History

PDF Solutions was incorporated in Pennsylvania in November 1992, and we reincorporated in California in November 1995. In July 2000, we reincorporated in Delaware and in July 2001, we completed an initial public offering. Our shares of common stock are currently traded on NASDAQ Global Market. From 2000 through 2009, we expanded our technology footprint and our operations in various countries through acquisitions. From 2009 to the present, we have primarily focused on the pervasive application of our technology to leading edge logic manufacturing and achieving yield targets with our clients to maximize Gainshare performance incentive revenues. Headquartered in San Jose, California, PDF Solutions operates worldwide with additional entities and/or offices in Canada, China, France, Germany, Italy, Japan, Korea, Singapore, and Taiwan.

Industry Background

Rapid technological innovation, with increasingly shorter product life cycles, now fuels the economic growth of the semiconductor industry. IC companies historically ramped production slowly, produced at high volume once products gained market acceptance, and slowly reduced production volume when price and demand started to decrease near the end of the products' life cycles. Now, companies often need to be the first to market and the first to sell the most volume when a product is first introduced so that they have performance and pricing advantages over their competition, or else they lose market opportunity and revenue. Increased IC complexity and compressed product lifecycles create significant challenges to achieve competitive initial yields and optimized performance. For example, it is not uncommon for an initial manufacturing run to yield only 20%, which means that 80% of the ICs produced are wasted. Yield improvement and performance optimization are critical drivers of IC companies' financial results because they typically lead to cost reduction and revenue generation concurrently, causing a leveraged effect on profitability.

Technology and Intellectual Property Protection

We have developed proprietary technologies for yield simulation, analysis, loss detection, and improvement. The foundation for many of our solutions is our CV infrastructure ("CV*i*") that enables our customers to electrically characterize the manufacturing process, and establish fail-rate information needed to calibrate manufacturing yield models, prioritize yield improvement activities and speed-up process learning-cycles. Our CV*i* includes proprietary Characterization Vehicle® test chips, including designs of experiments and layout designs, and a proprietary and patented highly parallel electrical functional and parametric-test system, comprised of hardware and software designed to provide an order-of-magnitude reduction in the time required to test our Characterization Vehicle® test chips. In addition, our technology embodies many algorithms, which we have developed over the course of many years, and which are implemented in our products including Exensio™, *data*POWER®, pdCV™, Maestria®, and Library Analyzer™, among others. Further, our IP includes methodologies that our implementation teams use as guidelines to drive our customers' use of our CV® test chips and technologies, quantify the yield-loss associated with each process module and design block, simulate the impact of changes to the design and/or to the manufacturing process, and analyze the outcome of executing such changes. We continually enhance our core technologies through the codification of knowledge that we gain in our solution implementations.

Our future success and competitive position rely to some extent upon our ability to protect these proprietary technologies and IP, and to prevent competitors from using our systems, methods, and technologies in their products. To accomplish this, we rely primarily on a combination of contractual provisions, confidentiality procedures, trade secrets, and patent, copyright, mask work, and trademark laws. We license our products and technologies pursuant to non-exclusive license agreements that impose restrictions on customers' use. In addition, we seek to avoid disclosure of our trade secrets, including requiring employees, customers, and others with access to our proprietary information to execute confidentiality agreements with us and restricting access to our source code. We also seek to protect our software, documentation, and other written materials under trade secret and copyright laws. As of December 31, 2013, we held 63 U.S. patents, Our issued patents have expiration dates through 2032. We intend to prepare additional patent applications when we feel it is beneficial. Characterization Vehicle®, CV®, *data*POWER®, Maestria®, pdFasTest®, PDF Solutions®, the PDF Solutions logo, Yield Ramp Simulator®, and YRS® are registered trademarks of PDF Solutions, Inc. or its subsidiaries, and Design-to-silicon-yield™, *dP*-bitMAP™, *dP*-Defect™, *dP*-Mining™, *dP*-SSA™, *dP*-Variability Analysis™, *dP*-WorkFlow™, Exensio™, Library Analyzer™, VSF™, pdCV™, Template™, and YieldAware™-FDC are our common law trademarks

Products and Services

Our solutions consist of integration engineering services, proprietary software, and other technologies designed to address our customers' specific manufacturing and design issues.

Services and Solutions

Manufacturing Process Solutions ("MPS"). The IC manufacturing process typically involves four sequential phases: research and development to establish unit manufacturing processes, such as units for the metal CMP or lithography processes; integration of these unit processes into functional modules, such as metal or contact modules; a yield ramp of lead products through the entire manufacturing line; and volume manufacturing of all products through the life of the process. We offer solutions targeted to each of these phases designed to accelerate the efficiency of yield learning by shortening the learning cycle, learning more per cycle, and reducing the number of silicon wafers required. Our targeted offerings include:

- *Process R&D:* Our process R&D solutions are designed to help customers increase the robustness of their manufacturing processes by characterizing and reducing the variability of unit processes and device performance with respect to layout characteristics within anticipated process design rules.

- *Process Integration and Yield Ramp:* Our process integration and yield ramp solutions are designed to enable our customers to more quickly ramp the yield of new products early in the manufacturing process by characterizing the process-design interactions within each key process module, simulating product yield loss by process module, and prioritizing quantitative yield improvement by design block in real products.

Volume Manufacturing Solutions ("VMS"). Our volume manufacturing solutions are designed to enable our customers to extend our yield ramp services through the life of the process by continuing to collect test data and equipment signals during production and improving yield while reducing the overhead of manufacturing separate test wafers. Our Exensio™ YieldAware™ solution combines software and services to enable customers to collect and combine product test data and equipment signals during production to improve yield while simultaneously reducing the overhead of manufacturing.

Design-for-Manufacturability ("DFM") Solutions. Our DFM solutions are designed to enable our customers to optimize yields, improve parametric performance, and reduce product ramp time by integrating manufacturability considerations into the design cycle before a design is sent to the mask shop to more quickly and cost-effectively manufacture IC products. We target these solutions to customers' requirements by providing the following:

- *Logic DFM Solutions:* Logic DFM solutions include software, IP, CV® infrastructure, and services designed to validate customers' process design kit (PDK) and to maximize functional and parametric yield improvements while achieving requirements for density or performance, for example, in the logic portions of an IC design. A CV® test chip optimized to the design style of an IC design provides any necessary design-specific parametric and functional yield models for the design style. Our software helps designers optimize the yield of the logic portion by using process-specific and design style-specific yield models and technology files that enable identification and implementation of IP design building block improvements that result in enhanced yield.

- *Circuit Level DFM Solutions:* Circuit level DFM solutions include software and services designed to anticipate the effects of process variability during analog/mixed signal/RF circuit design to optimize the manufacturability of each block given a pre-characterized manufacturing process.

- *Memory DFM Solutions:* Memory DFM solutions include software and services designed to optimize the memory redundancy and bit cell usage given a pre-characterized manufacturing process.

- *Template™ Technology Physical IP Solutions:* Template™ physical IP solutions include Library Analyzer™ software and IP for first identifying and developing a set of layout patterns that are optimized to a given manufacturing process and target product application and second checking proposed product layout designs against this set of patterns for optimal manufacturability. A complete characterization of all transistor and layout patterns used in these Template™ layouts can be performed with the CV® infrastructure. These Template™ layouts serve as the building blocks for design organizations to construct standard cell libraries and larger physical IP blocks.

Products

Our Manufacturing Process, Volume Manufacturing, and DFM solutions incorporate the use of various elements of our software products and other technologies, depending on the customers' needs. Our software products and other technologies include the following:

Characterization Vehicle® Infrastructure. Our test chip design engineers develop a design of experiments ("DOEs") to determine how IC design building blocks interact with the manufacturing process. Our CV® software utilizes the DOE, as well as a library of building blocks that we know has potential yield and performance impact, to generate CV® test chip layouts. Our CV® infrastructure includes:

- *CV® Test Chips.* Our family of proprietary test chip products is run through the manufacturing process with intentional process modifications to explore the effects of potential process improvements given natural manufacturing variations. Our custom-designed CV test chips are optimized for our test hardware and analysis software and include DOEs tuned to each customer's process. Our full-reticle short-flow CV® test chips provide a fast learning cycle for specific process modules and are fully integrated with third-party failure analysis and inspection tools for complete diagnosis to root cause. Our Scribe CV® products are inserted directly on customers' product wafers and collect data from product wafers about critical layers. Our "direct probe" CV® test chips enable ultra fast yield learning for new product designs by allowing our clients to measure components of actual product layout.

- *pdCV™ Analysis Software.* Our proprietary software accumulates data from our CV® test chips, enabling models of the performance effects of process variations on these design building blocks to be generated for use with our Yield Ramp Simulator software.

- *pdFasTest® Electrical Wafer Test System.* Our proprietary system enables fast defect and parametric characterization of manufacturing processes. This automated system provides parallel functional testing, thus minimizing the time required to perform millions of electrical measurements to test our CV® test chips.

Yield Ramp Simulator® (YRS®) Software. Our YRS software analyzes an IC design to compute its systematic and random yield loss. YRS software allows design attribute extraction and feature-based yield modeling. YRS® software takes as input a layout that is typically in industry standard format and proprietary yield models generated by running and testing our CV® test chips. YRS® software is designed to estimate the yield loss due to optical proximity effects, etch micro-loading, dishing in CMP, and other basic process issues.

Template™ Technology. Our Template™ technology includes Library Analyzer™ software and IP for identifying and developing a set of layout patterns that are tailored to a given manufacturing process and target product application and checking proposed designs against this set of patterns for optimal manufacturability.

Exensio™ YieldAware™ Enterprise Platform. Our Exensio™ YieldAware™ platform links across YMS, FDC, and other factory-wide data types, including in-line and end-of-line metrology, yield, performance and tool level sensor data, and links across factories. This enables sensor level root cause diagnosis of yield and performance issues that impact manufacturing, through building process models of these relationships. These on-line models then enable proactive optimization decisions for process control, process adjustments, PM scheduling, tool corrective actions, and wafer dispatching. The in-line, real-time decision-making based on the models is designed to reduce product variability and cost simultaneously. Our Exensio YieldAware platform also enables more rapid diagnosis and understanding of yield loss and performance-limiting mechanisms identified at both in-line and end-of -line wafer processing, through application of the developed models.

dataPOWER® YMS Software. Our *data*POWER® YMS software can be leveraged into the Exensio™ YieldAware™ platform or used standalone to collect yield data, load and store it in an analysis-ready database, which enables product engineers to identify and analyze production yield, performance, reliability and other issues. Our YMS software is designed to handle very large data sets, to efficiently improve productivity, yield and time-to-market at our customers' sites. *data*POWER® VSF™ software contains powerful visualization and reporting tools, which provide flexibility to address our customers' requirements. The *data*POWER® VSF™ Advanced Module includes extra proprietary yield analysis software tools that aid in the diagnosis of more complex yield issues. This includes defect analysis (*dP*-Defecttm) tools, memory analysis (*dP*-bitMAPtm), spatial signature analysis (*dP*-SSAtm) and data-mining (*dP*-Miningtm) tools. Finally, *data*POWER® VSF™ Automation and Reporting module enables web-based visualization of analysis templates, as well as an engine to drive the automation of actions and reports.

Maestria® FDC Software. Our Maestria® software can be leveraged into the Exensio™ YieldAware™ platform or used standalone to provide FDC capabilities for monitoring and alarming of manufacturing tool sets. These capabilities include analyzing tool sensor trace data and summary indicators to rapidly identify sources of process variations and manufacturing excursions. This is achieved by monitoring these equipment parameters through proprietary data collection and analysis features.

With the exception of *data*POWER® and Maestria®, the primary distribution method for our software and technologies is through our manufacturing process and volume manufacturing solutions although, we have in the past and may in the future separately license these and other technologies. Though *data*POWER® and Maestria® are primarily licensed separately, they may also be distributed within these solutions.

Customers

Our current customers are foundries, integrated device manufacturers ("IDMs"), and fabless semiconductor design companies. Our customers' targeted product segments vary significantly, including microprocessors, memory, graphics, image sensor solutions, and communications. We believe that the adoption of our solutions by such companies for usage in a wide range of products validates the application of our Design-to-silicon-yield solutions to the broader semiconductor market.

Global Foundries Inc. ("Global Foundries"), Samsung Electronics ("Samsung") and International Business Machines Corporation ("IBM") represented 33%, 24% and 17%, respectively, of our revenues for the year ended December 31, 2013. Global Foundries, IBM and Samsung represented 40%, 20% and 13%, respectively, of our revenues for the year ended December 31, 2012 and 24%, 19% and 15%, respectively, of our revenues for the year ended December 31, 2011. No other customer accounted for 10% or more of our revenues in 2013, 2012, and 2011.

Although a substantial portion of our total revenue is concentrated in a small number of customers, the total revenues for each of these customers in any period is the result of Design-to-silicon-yield solutions and Gainshare performance incentives revenues recognized in the period under multiple, separate contracts, with no interdependent performance obligations. These contracts were all entered into in the ordinary course of our business and contain general terms and conditions that are standard across most of our yield improvement solutions customers, including providing services typically targeted to one manufacturing process node, for example the 28 or 20 nanometer node. With respect to two of these customers, a portion of the total revenue attributable to them is pursuant to contracts that provided a general framework for services across multiple manufacturing process nodes. These multiple-node contracts also provide agreement as to the expected timing of delivery of services for some of the customers' process nodes. Under the multiple-node contract with one of these customers, the timing of delivery of services could change based on the customer's requirements and mutual agreement between us and the customer, however, the total revenue consideration, contract deliverable and labor hours required to deliver the services remain fixed. Accordingly, we recognize revenue under this contract as services are performed using the cost-to-cost percentage of completion method of contract accounting. The multiple-node contract with the other of these two customers provides a minimum quarterly resource commitment and a fixed price per quarter for each increment of resource. We mutually agree with the customer on a quarterly basis the resources, if any, that we will provide over the contractual minimum. The customer has the right under the contract to further reduce its quarterly resource commitment for a defined period, if and when, the customer's business is adversely impacted, based on contractually agreed terms. We recognize revenue from this contract under the proportional performance method in each quarter as services are performed. Based on the above, for both of these multiple-node contracts, we use the information available considering the minimum quarterly resource commitment and the timing of delivery of services for each calendar quarter for internal business planning purposes. Both of these multiple-node contracts also contain contingent variable fees. However, we do not depend on these fees for internal business planning because the potential Gainshare performance incentive revenue under the contracts is subject to many inherent risks, including our ability to achieve target performance objectives and future manufacturing volumes resulting in such Gainshare performance incentives. The Gainshare performance incentive revenue we recognize in any period is the result of many factors which are outside our control and are not known in advance of the acknowledgement of the Gainshare performance incentives amount we receive from our customers. See the discussion in "Revenue Recognition" included in Part II, Item 7. "Management's Discussion and Analysis of Financial Condition and Results of Operations" for further information. Additional discussion regarding the risks associated with Gainshare performance incentives revenue can be found under Item 1A, "Risk Factors."

International revenues accounted for approximately 62% of our total revenues for the year ended December 31, 2013 compared to 60% for the year ended December 31, 2012 and 68% for the year ended December 31, 2011. We base these calculations on the geographic location of where the work is performed. Additional discussion regarding the risks associated with international operations can be found under Item 1A, “Risk Factors”.

See our “Notes to Consolidated Financial Statements”, included under Part II, Item 8. “Financial Statements and Supplementary Data” for additional geographic information.

Sales and Marketing

Our sales strategy is to pursue targeted accounts through a combination of our direct sales force, our solution implementation teams, and strategic alliances. After we are engaged by a customer and early in the solution implementation, our engineers seek to establish relationships in the organization and gain an understanding of our customers’ business issues. Our direct sales and solution implementation teams combine their efforts to deepen our customer relationships by expanding our penetration across the customer’s products, processes and technologies. This close working relationship with the customer has the added benefit of helping us identify new product areas and technologies in which we should next focus our research and development efforts. We expect to continue to establish strategic alliances with process licensors, vendors in the electronic design automation software, capital equipment for IC production, silicon IP and mask-making software segments to create and take advantage of sales channel and co-marketing opportunities.

Research and Development

Our research and development focuses on developing and introducing new proprietary technologies, software products and enhancements to our existing solutions. We use a rapid-prototyping paradigm in the context of the customer engagement to achieve these goals. We have made, and expect to continue to make, substantial investments in research and development. The complexity of our Design-to-silicon-yield technologies requires expertise in physical IC design and layout, transistor design and semiconductor physics, semiconductor process integration, numerical algorithms, statistics and software development. We believe that our team of engineers will continue to advance our market and technological leadership. We conduct in-house training for our engineers in the technical areas, as well as focusing on ways to enhance client service skills. Although it fluctuates, we can have up to one quarter of our research and development engineers operating in the field, partnered with solution implementation engineers in a deliberate strategy to provide direct feedback between technology development and customer needs. Our research and development expenses were $13.3 million, $13.3 million and $14.0 million in 2013, 2012 and 2011, respectively.

Competition

The semiconductor industry is highly competitive and driven by rapidly changing design and process technologie